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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,289	12/28/2001	Young-Hun Ha	8733.560.00	2930

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EXAMINER	
DI GRAZIO, JEANNE A	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·D

Office Action Summary	Application No.	Applicant(s)	
	10/028,289	HA ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE 11 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-20,23 and 24* is/are pending in the application.

4a) Of the above claim(s) *9 and 12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,10,11,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims

Claims 1, 2, 4-8, 10-11 and 23-24 are pending with claims 1, 7 and 10 having been amended per Amendment of August 11, 2005. New claims 23 and 24 are added per Amendment of August 11, 2005. Claims 9 and 12-20 have been previously withdrawn per Applicant's election with traverse of Species A (claims 1-8 and 10-11 readable thereon) in the reply filed on May 21, 2004.

Applicant has also cancelled claims 3, 21 and 22 per Amendment of August 11, 2005.

Priority

Priority to Korean Patent Application No. 2000-85421 (Dec. 29, 2000) is claimed.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 11, 2005 has been entered.

Claim Objections

Claim 1 as amended objected to because of the following informalities:

Claim 1 as currently written is confusing. Applicant has presented a passivation layer towards the very beginning of the claim: "wherein a passivation layer is removed in the non-display region." Applicant then presents a passivation layer on the thin film transistor.

It may read as if there are two passivation layers; however, the Examiner believes that Applicant is claiming only one passivation layer.

Also, the passivation layer is removed in the non-display region.

The passivation layer is then removed in the pixel regions.

It seems as if there is no remaining passivation layer, although the Examiner presumes that Applicant is removing portions of the passivation layer in the pixel regions.

Appropriate correction is respectfully requested and required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent 6,204,907 B1 (to Hiraishi et al.).

As to claim 10 (amended), Hiraishi discloses, with reference to Figure 3, a lower substrate (11) having a display area and a non-display area of the lower substrate (11) an interlayer insulating film (9) (Applicant's "passivation layer") is removed in the periphery of the display (Applicant's "wherein a passivation layer is removed in the boundary region")(See also Column 10, Lines 51-55)(stating "[a] periphery of the display area, i.e., a part of the interlayer insulating film under a portion where the seal is provided is removed during the patterning of the interlayer insulating film in the same manner as the contact hole portion is removed."), a gate insulating layer formed (5) on the lower substrate (11) in the display area and the non-display area (the gate insulating film (5) extends into both peripheral and display regions), an upper substrate (20) having an area corresponding to the display area and the non-display area, the upper substrate (20) and the lower substrate (11) spaced apart and facing each other, a seal pattern of a constant thickness (14) formed between the upper substrate (20) and the lower substrate (11) along a boundary region between the display area and the non-display area.

Hiraishi explains that the liquid crystal can be thus smoothly injected (Column 10, Lines 39-40 and entire patent) and thus it may be inferred that the seal (14) must have an injection hole and that the liquid crystal is injected through the injection hole. It may thus also be inferred that once the liquid crystal is injected through the injection hole, the injection hole must then be sealed off to prevent liquid crystal matter from escaping through the injection hole. Please also note that the seal (14) contacts the gate insulating film (5).

Hiraishi also notes that *the thin film transistor is formed on the lower substrate, the thin film transistor having a drain electrode and a pixel electrode formed in a pixel region on the*

lower substrate, the pixel electrode connected to the drain electrode and the pixel electrode in contact with the gate insulating layer (Column 6, Lines 1-40).

Thus, claim 10 is rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4, 6-8, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,204,907 B1 (to Hiraishi et al.) in view of United States Patent 5,886,761 (to Sasaki et al.).

As to claim 1 (amended), 23 (new) and 24 (new), Hiraishi discloses, with reference to Figure 3, a lower substrate (11) including a seal pattern forming region between a display area and a non-display area of the lower substrate (11) wherein an interlayer insulating film (9) (Applicant's "passivation layer") is removed in the periphery of the display (Applicant's

"wherein a passivation layer is removed in the non-display region")(See also Column 10, Lines 51-55)(stating "[a] periphery of the display area, i.e., a part of the interlayer insulating film under a portion where the seal is provided is removed during the patterning of the interlayer insulating film in the same manner as the contact hole portion is removed."), a gate insulating layer (5) on the lower substrate (11) in the display area and the non-display area of the lower substrate (the gate insulating film (5) extends into both peripheral and display regions), an upper substrate (20), a seal pattern of a constant thickness (14) formed on the gate insulating layer (5) in a boundary between the display area and the non-display area of the lower substrate (11) and a liquid crystal layer (8) between the upper substrate (20) and the lower substrate (11).

The lower substrate (11) further includes gate wirings (1), a gate insulation film (5), a thin film transistor substrate (collectively 10), source wirings (2) and ITO therein (Column 10, Lines 26-35) and pixel electrodes (4).

Hiraishi does not appear to explicitly specify that *the display area includes a plurality of pixel regions and the passivation layer is removed in each of the plurality of pixel regions to thereby expose the gate insulating layer.*

Sasaki teaches and discloses a process for producing actively addressing substrate and liquid crystal display in which with reference to Figure 2, part of a passivation layer is removed (9) and a gate insulating layer (3) is exposed.

It would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Hiraishi in view of Sasaki to reduce image-sticking and for improved quality of display (Abstract). Furthermore, the number of process steps can be reduced (Id.).

Thus, claims 1, 23 and 24 are rejected.

As to claim 2, Hiraishi features the lower substrate (11) as having an insulative substrate (this is the TFT substrate). The insulative substrate extends across the display area and the non-display area.

Thus, claim 2 is rejected.

As to claim 4, the upper substrate includes a color filter substrate and opposite electrodes (6).

Thus, claim 4 is rejected.

As to claim 6, Hiraishi further has spacers (7 and 13).

Thus, claim 6 is rejected.

As to claims 7 (amended) and 8, Applicant's recited method steps of fabricating a liquid crystal panel for liquid crystal display devices would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made in view of the device as recited and taught by Hiraishi in view of Sasaki.

Thus, claims 7 and 8 are rejected.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,204,907 B1 (to Hiraishi et al.) in view of United States Patent 5,886,761 (to Sasaki et al.) and further in view of United States Patent 6,336,331 B1 (to Sakamoto et al.).

As to claim 5, Hiraishi does not appear to explicitly specify that the passivation layer is removed during a photolithographic mask step for simultaneous patterning of an active layer and the passivation layer.

Sakamoto teaches and discloses an active matrix liquid crystal display device having improved terminal connections in which an organic film and passivation film are patterned simultaneously (Column 3, Lines 50-55). Such simultaneous patterning results in a good contact between a terminal and a TAB in an active matrix substrate (Id.) and results in improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Sakamoto is evidence that ordinary workers in the field of liquid crystal would have found the reason, suggestion, and motivation to simultaneously pattern an organic film and passivation film for good contact between a terminal and a TAB in an active matrix substrate (Id.) and for improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystal at the time the invention was made to modify Hiraishi in view of Sakamoto for good contact between a terminal and a TAB in an active matrix substrate (Id.) and for improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Thus, claim 5 is rejected.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,204,907 B1 (to Hiraishi et al.) in view of Japanese Patent Application 02-220032 (to Obara et al.).

As to claim 11, Hiraishi does not appear to explicitly specify that the seal pattern is formed by a screen-printing process using thermosetting resin that includes glass fiber.

Obara teaches and discloses an electro-optic device wherein a thermosetting epoxy resin is used as a seal, the thermosetting epoxy resin is made by screen-printing and contains glass fiber spacers for seal strength and uniformity (Abstracts).

Obara is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion, and motivation to form a thermosetting seal with glass fibers by screen printing for seal strength and uniformity.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Hiraishi in view of Obara for seal strength and uniformity.

Thus, claim 11 is rejected.

Response to Arguments

Applicant did not present substantive arguments.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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JDG

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PRIMARY EXAMINER